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**DIVISIONAL  
APPLICATION  
FOR  
UNITED STATES  
LETTERS PATENT**

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**FOR:**                   **CLOCK MONITORING APPARATUS**  
**DOCKET NO.:**       **283579/01 DIV**

# Clock monitoring apparatus

## BACKGROUND OF THE INVENTION

### Field of the Invention

5           The present invention relates to a clock monitoring apparatus, particularly to a clock monitoring apparatus controlling a main clock and a sub clock to substitute for each other in failure to thereby realize a stable operation of a microcomputer even when the main clock is stopped.

10

### Description of the Prior Art

          Although a monitoring circuit of a clock is used for realizing a stable operation of a microcomputer, when a main clock is stopped, CPU is also stopped and therefore, it is requested for the monitoring circuit to monitor the clock by a signal stably operating even when the main clock is stopped and, when the main clock is stopped, to swiftly deal therewith.

15           In order to meet the request, it has been proposed that when the main clock is stopped, the stop of the clock is dealt with by switching the main clock to a sub clock as disclosed in, for example, a prior application (Single chip microcomputer: Japanese Patent Laid-Open No. 7-6155) and a method disclosed in the prior art literature is shown in FIG. 12.

25           In a circuit shown in FIG. 12, it is assumed that a main clock 1102 selected by a system clock switching circuit 1009 is oscillated normally. A timer 1004 is for counting a sub

clock 1101 and during a time period in which the main clock 1102 is normally oscillated, the sub clock 1101 is reset periodically before overflowing by a timer reset signal 1105 outputted from an internal bus 1201 by receiving execution  
5 of instruction in CPU. Therefore, the timer 1004 is not overflowed and therefore, a timer carry signal 1106 is not issued.

When the main clock 1102 is stopped, since the timer reset signal 1105 is not issued, the timer is overflowed, the  
10 timer carry signal 1106 is issued and a clock switch flag 1006 is changed. Thereby, a clock switch signal 1108 is issued and the main clock 1102 is switched to the sub clock 1101.

As described above, according to the prior art, when the main clock is stopped for some cause, the stop is dealt  
15 with by switching the main clock to the sub clock and there is not provided a constitution of spontaneously issuing a reset signal and initializing the clock as in the present invention. Therefore, when the main clock is stopped, the main clock is switched to the sub clock which continues operating in a state  
20 as it is and there is a drawback that in order to recover an original state, a control or the like by a software is separately needed. Further, since the normally-counted signal is the sub clock, much time is needed until the counter overflows, as a result, there also poses a problem of producing time lag  
25 until the stop is deal with (switch to sub clock). When the sub clock is stopped, the abnormal stop cannot be detected.

#### BRIEF SUMMARY OF THE INVENTION

## Objects of the Invention

It is an object of the present invention to provide a clock monitoring apparatus capable of automatically initializing a main clock when the main clock is stopped and continuing operation in a state before abnormality when the  
5 main clock is recovered, continuing operation by switching the main clock to a sub clock when the main clock cannot be recovered and issuing a flag when the sub clock is also stopped to thereby achieve stable operation of a microcomputer even  
10 when the main clock is stopped.

## Summary of the Invention

According to an aspect of the invention, there is provided a clock monitoring apparatus comprising a main clock monitoring  
15 portion including a first counter for counting a main clock, issuing a normal operation confirming flag indicating that a normal operation is being carried out when the first counter is overflowed or reaches a previously determined set value, monitoring the normal operation confirming flag by a sub clock,  
20 issuing a first main clock stop flag having an output in correspondence with H (high level) / L (low level) of the normal operation confirming flag and a main clock initializing signal for initializing the main clock when the main clock is determined to stop and resetting the first main clock stop flag when the  
25 main clock is recovered by receiving the main clock initializing signal, and a sub clock switching control portion including a second counter for counting a signal output produced by

calculating a logical sum of the sub clock and the first main clock stop flag at fall of the sub clock at a time point of generating the first main clock stop flag, switching to a sub clock operation by issuing a sub clock switching signal when  
5 a second counter output is overflowed or reaches a previously determined set value and resetting the second counter output when the main clock is recovered and a second main clock stop flag produced by inverting the first main clock stop flag and delaying the sub clock by a predetermined period by a main  
10 clock monitoring portion, is reset.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The above-mentioned and other objects, features and advantages of this invention will become more apparent by  
15 reference to the following detailed description of the invention taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a block diagram showing a first embodiment of a clock monitoring apparatus according to the invention;

20 FIG. 2 is a diagram showing a clock monitoring system constituted by a main microcomputer and a sub microcomputer including a clock monitoring apparatus according to the invention;

FIG. 3 is a block diagram showing a detailed constitution  
25 of the clock monitoring apparatus of FIG. 1;

FIG. 4 is a timing chart showing a waveform of operation in the case in which a main clock is stopped when a main clock

normal operation confirming flag is 0 and thereafter recovered;

FIG. 5 is a timing chart showing a waveform of operation in the case in which the main clock is stopped when the main clock normal operation confirming flag is 1 and thereafter  
5 recovered;

FIG. 6 is a timing chart showing a waveform of operation in the case in which the main clock is stopped and switched to a sub clock;

FIG. 7 is a timing chart showing a waveform of operation  
10 when an all clock stop flag is produced;

FIG. 8 is a flowchart for explaining operation of the clock monitoring apparatus according to the invention;

FIG. 9 is block diagram showing a second embodiment of a clock monitoring apparatus according to the invention;

15 FIG. 10 is a block diagram showing a third embodiment of a clock monitoring apparatus according to the invention;

FIG. 11 is a block diagram showing a fourth embodiment of a clock monitoring apparatus according to the invention; and

20 FIG. 12 is a block diagram showing an example of a clock monitoring apparatus of a prior art.

#### DETAILED DESCRIPTION OF THE INVENTION

An explanation will be given of a first embodiment of  
25 a clock monitoring apparatus according to the invention in reference to the drawings. The clock monitoring apparatus according to the invention is integrated into a clock monitoring

system shown in FIG. 2. The system comprises a main microcomputer 301 and a sub microcomputer 302 and the clock monitoring apparatus is included to a side of the sub microcomputer 302. FIG. 1 is a block diagram showing a constitution of the clock monitoring apparatus and FIG. 3 is a block diagram showing a further detailed constitution of the clock monitoring apparatus.

In FIG. 1, a clock monitoring apparatus 200 includes a main clock monitoring portion 201 including a counter, a sub clock switching control portion 202 including a counter, and a sub clock self monitoring portion 203 including a delay adding circuit and an exclusive-OR circuit.

In details, as shown by FIG. 3, the clock monitoring apparatus 200 is constituted by a main clock monitoring circuit 401, a reset\_A1 flag generating circuit 402, a reset\_A2 flag generating circuit 403, a sub clock switch signal generating counter 404 and delay adding circuits 405 and 406. Here, the main clock monitoring portion 201 is constituted by the main clock monitoring circuit 401, the reset\_A1 flag generating circuit 402, the reset\_A2 flag generating circuit 403 and a logical sum circuit (OR gate) and the sub clock switching control portion 202 is constituted by a logical sum circuit (OR gate) and the sub clock switch signal generating counter 404.

The main clock monitoring circuit 401 counts a main clock by the included counter and issues a normal operation confirming flag no\_reset constituting "H" ("1", that is, signifying high level) indicating that normal operation is being carried out

when the counter is equal to a predetermined set value, or overflowed. The flag no\_reset is monitored at fall of a sub clock. The reset\_A1 flag generating circuit 402 issues a flag reset\_A1 constituting "H" when the no\_reset is "H" and "L" when the no\_reset is "L" ("0", that is, signifying low level). The reset\_A2 flag generating circuit 403 issues a main clock stop flag reset\_A2 inverting the flag reset\_A1 and delaying by a half period of the sub clock and issues a main clock initializing (main microcomputer resetting) signal. However, the reset\_A2 flag generating circuit 403 issues the signals only when the main clock is determined to stop. When the main clock is recovered by receiving the main clock initializing signal, the reset\_A2 flag generating circuit 403 continues operating as it is by resetting the main clock stop flag reset\_A2.

Next, an explanation will be given of operation of the clock monitoring apparatus having the above-described constitution in reference to FIG. 4 through FIG. 8. First, an explanation will be given of a case of normal operation.

The main clock is counted and there is generated the signal no\_reset constituting "H" when the counter is equal to the set value or overflowed by the counter. At rise of the sub clock, no\_reset=0 (step S101 of FIG. 8) and simultaneously, the counter is reset and counting of the main clock is started (notation 51 in FIG. 4).

When the main clock is equal to the set value of the counter or overflowed (Yes at step S102 of FIG. 8), no\_reset=1 (notation 52 in FIG. 4, step S110 of FIG. 8).



At fall of the sub clock, no\_reset=1 (step S111 of FIG. 8) and therefore, the reset\_A1 stays to be "H" and the main microcomputer reset signal is not issued (notation 53 in FIG. 4).

5       Next, an explanation will be given of a case in which the main clock is stopped, the main microcomputer is initialized, as a result, the main clock is recovered. When the main clock is stopped, the counter is not overflowed or does not reach the predetermined set value (No at step S102 of FIG. 8).  
10       Therefore, the flag no\_reset stays to be "L" and the reset\_A1 stays to be "H" (step S103 of FIG. 8). Further, even when a time period of stopping the main clock is a time period of "H" of no\_reset or a time period of "L" thereof, the main clock is operated without problem. As shown by FIG. 7, when the main  
15       clock is stopped during a time period from rise of no\_reset to fall of the sub clock thereafter, the main microcomputer reset signal is generated at fall of the sub clock one period thereafter (notation 54 in FIG. 4).

      In the case in which no\_reset=0 at fall of the sub clock,  
20       reset\_A1=0. There is generated the flag reset\_A2 constituted by inverting the reset\_A1 and delaying by a half period of the sub clock. Therefore, in this case, at rise of the sub clock, reset\_A2=1 (step S104 of FIG. 8). There is issued the main microcomputer reset signal generated by calculating a  
25       logical sum of reset\_A1 and reset\_A2 to the main microcomputer and the main microcomputer is initialized (notation 55 in FIG. 4, step S105 of FIG. 8).

At this occasion, counting of a signal "wait" constituted by calculating a logical sum of reset\_A1 and the sub clock is started by the sub clock switch signal generating counter (notation 56 in FIG. 4, step S107 of FIG. 8), the sub clock  
 5 switching signal is issued and the sub clock is operated (step S107 of FIG. 8). That is, the sub clock switching control portion 202 starts counting the sub clock at a time point of generating the main clock stop flag, issues the sub clock  
 10 switching signal when the counter is overflowed or reaches the set value and is switched to sub clock operation. When the main clock is recovered and the main clock stop flag is reset by the main clock monitoring portion, the counter is reset and the operation returns to a standby state.

When the main clock is recovered before the sub clock  
 15 switch signal generating counter is overflowed, the counter in the main clock monitoring circuit 401 is overflowed again and no\_reset=1 (notation 57 in FIG. 4, step S110 of FIG. 8).

In the case of no\_reset=1 at fall of the sub clock, reset\_A1=1, reset\_A2 becomes "L" at rise of the sub clock.  
 20 The sub clock switch signal generating counter is reset at fall of reset\_A2 and therefore, the operation is not switched to the sub clock (notation 58 in FIG. 4).

Next, an explanation will be given of a case in which even when the main clock is stopped and the main microcomputer  
 25 is initialized, the main clock stays to be stopped in reference to FIG. 6. After initializing the main microcomputer by the above-described procedure, there is counted an output of a

signal "wait" constituted by calculating the logical sum of reset\_A1 and the sub clock by the sub clock switch signal generating counter (notation 61 in FIG. 4).

When the main clock is not recovered (notation 62 in FIG. 4), the sub clock switch signal generating counter is overflowed and the sub clock switching signal is issued (notation 63 in FIG. 4).

Further, an explanation will be given of a case in which after switching the operation clock to the sub clock, the sub clock is stopped in reference to FIG. 3 and FIG. 7. The sub clock self monitoring portion 203 is provided with the delay adding circuit 405 issuing a signal B constituted by delaying the sub clock by  $3/8$  period and the delay adding circuit 406 issuing a signal C produced by delaying the signal B by  $3/8$  period, functions when the main clock stop flag is generated and issues a flag indicating that all the clocks are stopped when the sub clock is stopped. By the function, it is possible that when the main clock is stopped, the main clock is automatically initialized and when the main clock is recovered thereby, the continuing operation is carried out under a state before abnormality. Further, it is possible that when the main clock cannot be recovered, the continuing operation is carried out by switching the main clock to the sub clock and when the sub clock is also stopped, the flag is issued. That is, the sub clock is provided with a function of monitoring the sub clock per se.

A specific explanation will be given of operation of

the sub clock self monitoring portion 203 as follows. Notation "A" in FIG. 3 designates the sub clock, notation "B" designates the clock produced by delaying the sub clock by  $3/8$  period and notation "C" designates the clock produced by delaying "B" by  $3/8$  period.

When the main clock is stopped (step S108 of FIG. 8), reset\_A2 in FIG. 3 is "H" and therefore, AND of reset\_A2 and an inverted signal of a signal produced by calculating exclusive-OR of A, B, and C, constitutes all clock stop flag.

10 When the sub clock is stopped, after  $3/4$  period, the all clock stop flag is issued (step S109 of FIG. 8). The flag can be issued even when the sub clock is stopped in the state of "H" or the state of "L". Further, the delay of  $3/8$  period is added in generating "B" and "C" because it is determined that the

15 phase relationship is mostly pertinent for preventing occurrence of spike and even when the value of delay is changed, the change naturally falls in the range of the invention.

An explanation will be given of a second embodiment of a clock monitoring apparatus according to the invention as

20 follows. According to the embodiment, as shown by FIG. 9, the sub clock self monitoring portion is deleted in the above-described first embodiment. Although the all clock stop flag cannot be issued thereby, since the delay adding circuits and the exclusive-OR circuit are dispensed with, the circuit

25 scale can be reduced.

An explanation will be given of a third embodiment of a clock monitoring apparatus according to the invention as

follows. According to the embodiment, as shown by FIG. 10, there is added a main clock temporarily stopping signal for controlling to issue the main microcomputer reset signal, the sub clock switching signal and the all clock stop flag of the above-described first embodiment. Thereby, even when the user intentionally stops the main clock by a signal of temporarily stopping the main clock such as HALT, the respective output signals are not issued.

An explanation will be given of a fourth embodiment of a clock monitoring apparatus according to the invention as follows. According to the embodiment, as shown by FIG. 11, the sub clock switching control portion of the above-described first embodiment is provided with a sub microcomputer reset signal generating function. Thereby, after switching to a sub clock operation mode, the sub microcomputer per se can be initialized by a sub microcomputer reset signal generated via a delay circuit.

In this way, the invention realizes that when the main clock is stopped, the main clock is initialized and when the main clock is recovered thereby, the continuing operation is carried out under the state before abnormality. Further, when the main clock is not recovered, the continuing operation can be carried out by switching the main clock to the sub clock. Further, when the sub clock is also stopped, the all clock stop flag can be issued, further, a series of operation can be carried out without control of a software or the like.

Further, although the normally counting signal for

monitoring the operational state of the main clock has been the sub clock in the example of the related art, according to the invention, the signal is constituted by the high-speed main clock and therefore, a time period until the counter is  
5 overflowed or reaches the set value, is shortened and in comparison with the example of the related art, there is also achieved an effect of capable of significantly shortening a time period until dealing with the stop of the main clock.

Further, in the above-described embodiments, various  
10 modifications can be carried out such as replacing the main microcomputer to a main clock generating apparatus, replacing the sub microcomputer to a system including the circuit of the invention, further, using the main microcomputer initializing signal, the sub clock switching signal and the  
15 all clock stop flag by themselves, or using these by various combinations.

Although the invention has been described with reference to specific embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the  
20 disclosed embodiments will become apparent to persons skilled in the art upon reference to the description of the invention. It is therefore contemplated that the appended claims will cover any modifications or embodiments as fall within the true scope of the invention.